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A cost roadmap for silicon heterojunction solar cells

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ABSTRACT

Research and development of silicon heterojunction (SHJ) solar cells has seen a marked increase since the recent expiry of core patents describing SHJ technology. SHJ solar cells are expected to offer various cost benefits compared to conventional crystalline silicon solar cells. This paper analyses the production costs associated with five different SHJ cell designs, including an interdigitated back-contacted (IBC) design. Using life-cycle costing, we analyzed the current cost breakdown of these SHJ designs, and compared them to conventional diffused junction monocrystalline silicon modules. Coupling the results for current designs with literature data on technological improvements, we also present a prospective analysis of production costs for the five SHJ cells and modules.

For current designs, module costs were calculated to be 0.48–0.56 USD per Watt-peak (W_p) for SHJ modules, compared to 0.50 USD/W_p for a conventional c-Si module. The efficiency bonus for SHJ modules compared to conventional c-Si modules is offset by a strong increase in metallization costs for SHJ designs, as comparatively large amounts of low-temperature silver-paste are required. For module materials, the requirement for conductive adhesives results in a small cost penalty for SHJ modules compared to c-Si modules, which is more than balanced by the effect of higher efficiency in SHJ modules.

Our prospective study showed that improvements in cell processing and module design could result in a significant drop in production costs for all module types studied. The SHJ modules gain much advantage by reducing and replacing silver consumption, increased cell efficiency and thinner wafers and have prospective production costs of 0.29–0.35 USD/W_p. Conventional c-Si module cost is less sensitive to silver paste consumption, limiting the potential for cost reduction, and has prospective production costs of 0.33 USD/W_p. Replacement of indium-tin-oxide was not found to contribute substantially to a reduction in module costs.

1. Introduction

Concurrently with the strong growth in PV module production and sales, average PV module prices have dropped sharply over the last decade. Polysilicon, wafer, cell and module prices dropped especially sharp over the last few years, as shown in Fig. 1. In the Netherlands, PV module prices including tax dropped by almost 50% between 2011 and 2013, from 2 EUR per W_p to 1.13 EUR per W_p [1], while global spot prices (excluding tax) for PV modules have dropped to 0.6 USD/W_p (see Fig. 1). Price decreases have long been following a learning curve that has been valid for multiple decades, however, more recently, due to decreased demand and resulting oversupply, prices have dropped below what could be extrapolated from the learning curve. As a result, PV producers are scrambling for opportunities to reduce production costs. On the other hand, although residential grid parity has been reached in several countries worldwide [2], PV electricity is as of yet not competitive with fossil electricity generation [3–7]. These two factors emphasize the need for further cost reductions in the PV industry, in order to assure PV production that is financially sustainable and competitive with bulk electricity generation.

Photovoltaic systems offer us the possibility to produce electricity with low emissions of greenhouse gasses [9–13], low energy pay-back time, and low emissions of toxic or otherwise harmful substances, compared to traditional forms of electricity production. Its' modular nature allows for the application on a variety of scales, from small-scale decentralized and off-grid to large-scale, centralized electricity production. According to International Energy Agency's World Energy Outlook, PV will contribute significantly to a sustainable energy supply system [14]. Because of this expectation, adoption of PV is being supported by national

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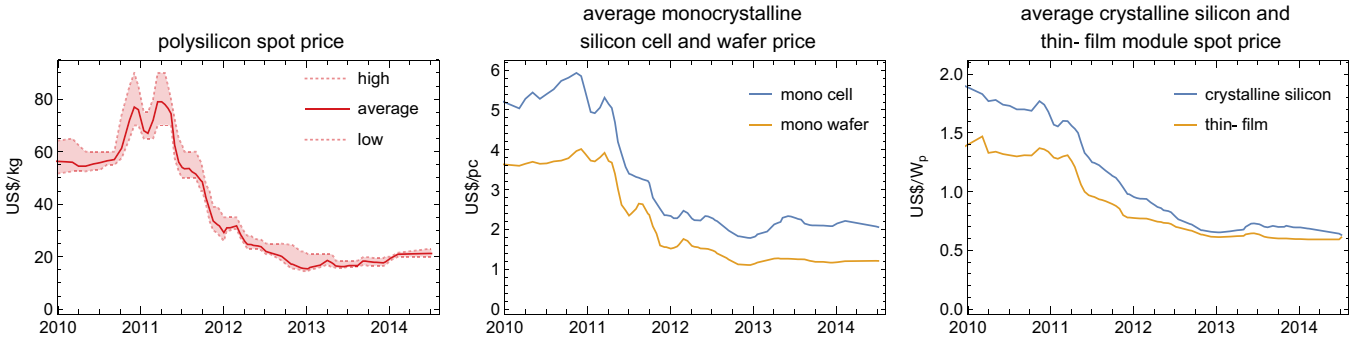

Fig. 1. Overview of development of prices for polysilicon (left, in USD/kg), monocrystalline cells and wafers (middle, USD/W_p) and crystalline silicon and thin film modules (right, USD/W_p). Data: [8].

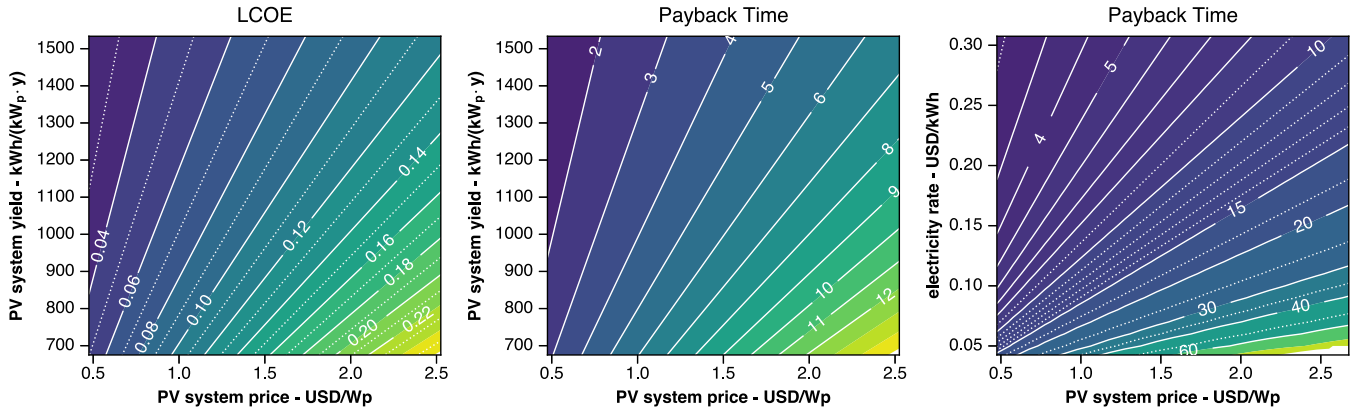

Fig. 2. Left: effect of PV system price and PV system yield on the levelised cost of electricity from a PV system. Middle: effect of PV system price and PV system annual yield on the investment payback time of a PV system, based on an electricity rate of 0.26 USD/kWh. Right: effect of PV system price and electricity price on the payback-time of a PV system, at a yield of 875 kWh/k W_p.

governments worldwide, at sometimes high financial costs for society [15]. Cost reductions are thus of substantial societal importance when deployment of solar energy covers larger shares of total electricity generation.

In order for PV to become a competitive source of electricity production, the levelized cost of electricity (LCOE) from PV should decrease below residential electricity prices ("socket parity") and below wholesale electricity prices ("grid parity"). Furthermore, for PV to become a viable investment option for both consumers and businesses, the payback time (PBT) of investing in PV should drop to about 3–5 years [16]. Fig. 2 shows the effect of PV system price and annual yield on LCOE and PBT. From this figure, we can deduce that, in order for PV to reach grid parity (instead of the already achieved socket parity) PV system prices still need to drop significantly. For PV to compete with combined-cycle natural gas and coal with a levelized cost of electricity (LCOE) of about 0.05 USD/kWh [17], we estimate that PV system prices need to drop below 0.60–1.00 USD/W_p, thus PV module prices should drop below 0.3–0.5 USD W_p[1]

For a large part, cost reductions in PV production have been achieved due to economies of scale, and technological learning in the PV production supply chain [18]. More recently we have seen an increased focus on intrinsic cost reductions. General approaches for cost reductions have traditionally been to decrease material use or replace expensive materials with cheaper ones. For instance, silicon consumption per watt-peak (W_p) has decreased significantly due to increased efficiencies and the use of increasingly thin wafers, while silver use for metallization has also decreased over the years. Significant cost reductions have been obtained with this approach, however, more recently the room for further improvement has decreased. This has resulted in a variety of approaches being researched, including a shift from the traditional diffused junction crystalline PV devices, towards alternative designs or technologies.

One of those "new" technologies is the silicon heterojunction (SHJ) solar cell technology. SHJ solar cells are produced from silicon wafers in a low temperature process that does not exceed 200 °C. High temperature diffusion of the p-n junction is replaced with a low temperature deposition of a p-doped amorphous silicon layer on an n-type monocrystalline silicon wafer.

This technology is only produced on a large scale by Panasonic (by acquiring Sanyo), but a recent expiry of the core patents describing their SHJ technology has lead to a marked increase in R&D on this technology [19,20]. The large interest is mainly due to the fact that [19,20]: (**1**) SHJ fabrication is a simple process with high efficiency cells as a result; (**2**) the deposition of the thin film layers for SHJ cells can benefit from ample experience with these processes in the flat-display industry; (**3**) SHJ modules have a low temperature coefficient which leads to higher energy yields compared to conventional c-Si modules, and (**4**) SHJ cells benefit more from the application of thinner wafers, because the deposited thin-film layers allow for very good passivation of the wafer surface.

Current R&D mainly focuses on improving device performance, but novel design structures and processing steps are also being investigated, aiming to lower production costs. Examples are

[1] Assuming a PV system yield of 800–1400 kWh/(k W_p year) and a module-to-system price ratio of 2.

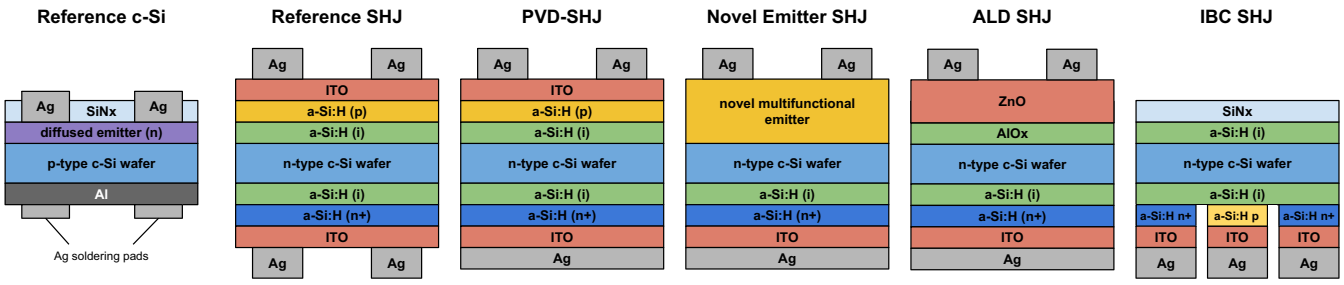

Fig. 3. Graphical representation of the current scenario cell designs analysed in this study. Based on designs from [13].

Table 1
Overview of design parameters for the current scenario cell designs. The abbreviations of the design names refer to the discussion of these designs in Section 2.1 and are also shown in Figs. 3 and 4.

Short name	Ref-cSi	Ref-SHJ	PVD-SHJ	NE-SHJ	ALD-SHJ	IBC-SHJ
Wafer type	p-type	n-type	n-type	n-type	n-type	n-type
Wafer thickness	180	180	180	180	180	180
Passivation		a-Si:H (i)	a-Si:H (i)	a-Si:H (i)	Al2O3	a-Si:H (i)
Emitter	diffused n-dopant	a-Si:H (p)	a-Si:H (p)	multifunctional layer	ZnO	a-Si:H (p)
TCO	-	ITO	ITO	ITO (back only)	ITO (back only)	ITO (back only)
Metallization front	Ag print	Ag print	Ag print	Ag print	Ag print	-
Metallization back	Al print with Ag soldering pads	Ag print	Ag PVD	Ag PVD	Ag PVD	Ag PVD
Cell area (cm^2)	239	239	239	239	239	239
Cell efficiency[a]	19.4%	22.4%	22.7%	19.7%	19.5%	23.3%
Module efficiency[a]	17.1%	19.7%	20.0%	17.3%	17.2%	20.5%

[a] Cell and module efficiencies are monofacial efficiencies.

alternative materials for the transparent conductive oxide (TCO), alternative metallization schemes and materials, and alternative passivation structures and materials [20]. Current SHJ cell designs rely on expensive materials (silver, indium) and processing steps.

In order to improve the economic performance of SHJ technology, the FLASH[2] programme investigates several alternative SHJ cell designs. The research focuses not only on replacement of expensive and high price volatility materials like indium (for the TCO) and silver (for metallization) but also on simplifying the production process.

In this paper we present an analysis of the cost structure of PV modules based on five different SHJ cell designs, and, as a reference, conventional diffused junction monocrystalline silicon PV cells. Furthermore, we use the results obtained to evaluate a roadmap towards significant cost reductions in prospective SHJ modules. With the analysis of current production costs, we aim to establish a baseline, but also to compare and rank different SHJ cell designs in terms of cost, and to provide an upfront cost estimation of these different cell designs while they are still under development. Together with previous work [13] focusing on the environmental performance of SHJ solar cells and modules, we aim to perform an ex-ante technological assessment of SHJ technology, and SHJ cell and module production on an industrial scale of designs currently in laboratory stage. To analyze where this technology could go in 10 years, we have also investigated a roadmap towards production of derivatives of the SHJ designs in 2025.

2. Methods

In a previous study we performed a life cycle assessment (LCA) of four of the five SHJ designs studied here, resulting in a detailed description of SHJ cell and module production [13]. LCA studies aim to establish the environmental impact of products, and are based on establishing a life cycle inventory (LCI): a detailed inventory of all material and energy inputs and waste outputs of production of a product. We used the life cycle inventory gathered in our previous study to perform a bottom-up cost analysis using life cycle costing (LCC), by attributing costs to all the material, energy and waste flows in the LCI. Some updates were made to our previous LCI. The LCI used in this study is shown, per processing step, in Tables A2–A7 in the appendix.

The methodology for LCA is firmly standardised, both in general terms [21,22] and for PV specifically [23]. For LCC, this methodology is not yet standardized [24], but in many ways very similar to LCA. We will follow the approach detailed by Rebitzer and Seuring [25] and Hunkeler and Rebitzer [26] for LCC, our previous study followed PV LCA guidelines by Fthenakis et al. [23].

2.1. Designs studied

In this study we compared the production of various different SHJ cell designs, and compared this with the production of a conventional crystalline silicon solar cell. The different designs studied here are shown in Figs. 3 and 4 and described in detail in Tables 1 and 2. We assumed that production with commercial scale (optimized for throughput) cell processing tools, with wafer throughputs of 3600 wafers/hr (or approximately 120–130 MW/yr dependent on cell efficiency). As in our previous work [13] we assumed that the designs to be based on a 180 µm monocrystalline Cz Si wafer, passivated with intrinsic amorphous silicon (a-Si:H) on both sides, deposited via plasma enhanced chemical vapor deposition (PECVD). The reference design (see Fig. 3) has a standard SHJ structure: an a-Si:H emitter and back surface field (BSF), and an indium-tin-oxide (ITO) transparent conductive oxide (TCO). Metallization is screen-printed silver on both sides. Compared to conventional silicon cells, more silver paste is required for the front grid due to the low-temperature curing process. As shown in [19], there is no single preferred metallization layout in SHJ

[2] The FLASH programme (acronym for FundamentaLs and Application of silicon heterojunction solar cells) is a Dutch research programme funded by technology foundation STW under their *Perspectief* programme. *Perspectief* programmes aim to employ fundamental technical research to apply novel technologies in society.

Table 2
Overview of design parameters for the prospective scenario cell designs. The abbreviations of the design names refer to the discussion of these designs in Section 2.1 and are also shown in Figs. 3 and 4.

Short name	Ref-cSi	Ref-SHJ	PVD-SHJ	NE-SHJ	ALD-SHJ	IBC-SHJ
Wafer type	p-type	n-type	n-type	n-type	n-type	n-type
Wafer thickness	**100**	**100**	**100**	**100**	**100**	**100**
Passivation		a-Si:H (i)	a-Si:H (i)	a-Si:H (i)	Al2O3	a-Si:H (i)
Emitter	diffused n-dopant	a-Si:H (p)	a-Si:H (p)	multifunctional layer	ZnO	a-Si:H (p)
TCO	–	**ZnO**	**ZnO**	**ZnO**	**ZnO**	**ZnO**
Metallization front	**Cu print**	**Cu plate**	**Cu plate**	**Cu plate**	**Cu plate**	–
Metallization back	Al print with **Cu soldering pads**	**Cu plate**	**Cu PVD**	**Cu plate**	**Cu plate**	**Cu plate**
Cell area (cm^2)	239	239	239	239	239	239
Cell efficiency[a]	**20.7%**	**25.4%**	**25.3%**	**23.2%**	**23.0%**	**25.9%**
Module efficiency[a]	**19.7%**	**24.1%**	**24.0%**	**22.1%**	**21.8%**	**24.6%**

[a] Cell and module efficiencies are monofacial efficiencies.

Table 3
Overview of estimated SHJ cell performance parameters and the assumptions behind their calculation. Method based on the approach in [18].

Cell parameter	Ref-SHJ	PVD-SHJ	NE-SHJ	ALD-SHJ	IBC-SHJ
current cell designs					
Open-circuit voltage (V)	0.737	0.737	0.729 −No ITO at front side + No TCO/a-Si:H interface	0.715 −negative effect of TCO on Voc −front emitter changed	0.744 + Reduced recombination at front interfaces
Short-circuit current density (mA/cm^2)	0.380	0.382 + Increased reflectivity backside metal	0.356 + decreased parasitic absorption of ITO −decreased lateral conductivity emitter/TCO	0.358 − decreased lateral conductivity emitter/TCO	0.389 + Elimination of shadowing front + Decreased parasitic TCO absorption front
Fill factor	0.800	0.808 +Increased conductivity backside metal	0.760 −decreased lateral conductivity emitter/TCO	0.761 −decreased lateral conductivity emitter/TCO	0.803 + High contact coverage back
Cell efficiency	22.4%	22.7%	19.7%	19.5%	23.3%
Module efficiency	20.2%	20.5%	17.8%	17.5%	21.0%
prospective cell designs					
Open-circuit voltage	0.760	0.760	0.756	0.746	0.768
Short-circuit current density	0.400	0.402	0.386	0.386	0.409
Fill factor	0.820	0.828	0.796	0.797	0.826
Cell efficiency	24.9%	25.3%	23.2%	23.0%	25.9%
Module efficiency	23.7%	24.0%	22.1%	21.8%	24.6%

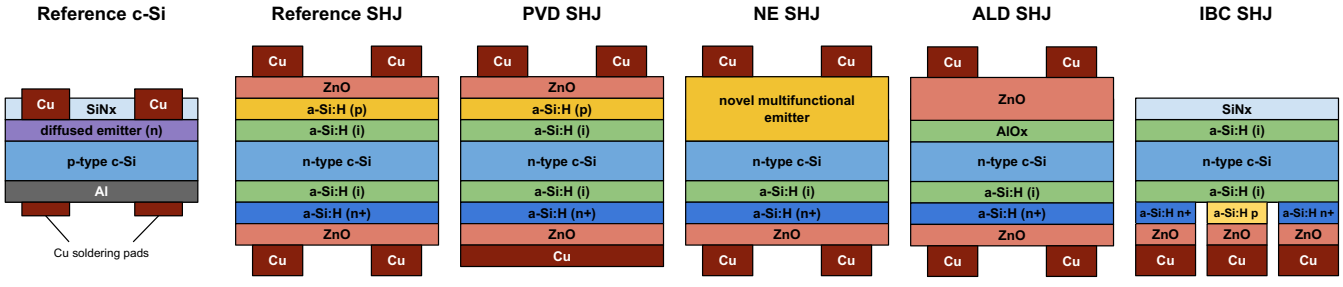

Fig. 4. Graphical representation of the prospective scenario cell designs analysed in this study. Based on designs from [13].

Table 4
Overview of general economic input parameters. FTE refers to full-time equivalent.

Parameter	Unit	Value	Source
Depreciation rate	–	8.0%	[18]
Cleanroom cost	USD/m^2a^{-1}	200	[18]
Skilled labor	USD/(FTE · a)	70,000	Own estimate
Unskilled labor	USD/(FTE · a)	50,000	Own estimate

Table 5
Main input parameters for Cz ingot production. Amounts per kg of Cz Silicon ingot produced.

Input	Amount	Unit	Source	Unit cost	Source
PV grade silicon	1.07	kg	[33]	16.47	Own model
Electricity (hydro)	85.6	kWh	[33]	0.025	[18]
Argon	5.8	kg	[33]	0.714	Own survey

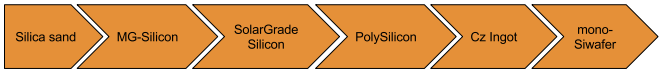

Fig. 5. Schematic overview of the silicon, ingot and wafer production chain studied here.

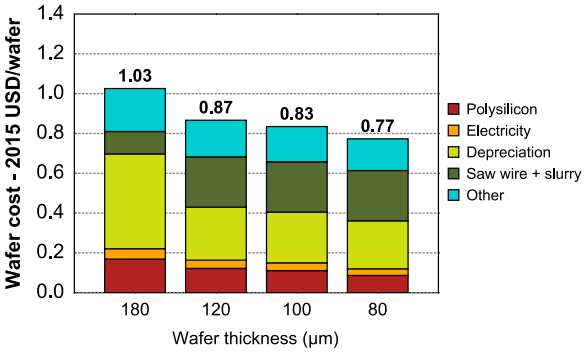

Fig. 6. Overview of wafer production costs for various wafer thicknesses. In this study, p-type and n-type wafers are assumed to have equal production costs.

research and development. Therefore, we have compared SHJ designs with different forms of metallization: the reference design with an Ag grid at the back (Ref-SHJ), and SHJ cells with a PVD deposited Ag layer at the back (PVD-SHJ).

Aside from these designs with only changes in metallization, we have studied three other designs: The Novel Emitter SHJ (NE-SHJ) design has no ITO or a-Si:H layers on the front, but instead has a multifunctional layer which aims to combine the function of passivation, emitter, TCO and antireflective coating in a single layer.

The atomic layer deposition design (ALD-SHJ) replaces the standard SHJ front side with a hole selective Al_2O_3/ZnO window layer. The aluminum oxide layer is deposited with ALD, while the zinc oxide layer is sputtered.

The final design studied is an interdigitated back contacted (IBC) SHJ cell (IBC-SHJ). The IBC structure is produced with masked plasma-deposition (PECVD) and -etching, while the contacts are formed at the back by masked PVD of ITO and silver.

We compared these five SHJ designs with a conventional c-Si cell, with a p-type wafer and diffused emitter, aluminum BSF, SiN_x anti-reflective coating (ARC) and fired-through silver grid at the front, and silver soldering pads at the back.

2.1.1. Cell design efficiencies

This study presents productions cost for five different SHJ cell designs. For most of these designs, it is difficult to assign an accurate cell efficiency, as they are not being produced and tested at a large scale. With an approach similar to that in [18] we have calculated cell efficiencies for each of the SHJ designs, based on an assumed cell efficiency of 22.4% for the reference SHJ design, adjusting the efficiency for each alternative design based on the effect of changes in the cell structure on open-circuit voltage (V_{oc}), short-circuit current (I_{sc}) and fill factor (*FF*). The assumed efficiencies for each of the SHJ designs, and the assumptions made for their calculations are shown in Table 3.

2.2. Scope of the study

The aim of the study reported here was to quantify production costs for the five SHJ cell designs mentioned in the previous section, show a roadmap towards reduction of these costs in the future, and make a comparison with conventional c-Si modules. With the analysis we hope to be able to offer an ex-ante production cost assessment of different SHJ designs currently being developed, in order to be able to steer the R&D towards cost reductions. Furthermore, we hope to identify the importance of SHJ specific design elements in cell and module production to overall costs.

Fig. 7 shows the cell production cycles we have analyzed, which are detailed below in Sections 3.1 and 3.2. The focus of our study was on production costs. We therefore established these costs for a functional unit defined as "one Watt of rated (peak) module power output" (USD/W_p). The aim of the study is to analyze these production costs based on a breakdown of the production cycles detailed in Fig. 7.

2.3. Cost data and calculations

The production costs for the designs studied were calculated by combining material and energy prices with a life cycle inventory (LCI) of cell production. The LCI gives a detailed bill of materials needed for production of the studied solar cells and modules. The LCI was taken from our previous work [13], while cost data was taken from a variety of sources. For an overview of input cost data, see Table A9 in the appendix. Some general cost data assumptions are given in Table 4.

The LCI data from our previous study [13], was gathered with the aim of analysing the environmental impact of solar cell production. Therefore, it is focused on material and energy in- an outputs, and emissions of harmful substances. As a result, it does not accurately reflect costs at all times. For instance, the price of silver and indium on the global market is not only a result of the materials and energy expended in acquiring them, but is also a reflection of the balance between the supply and demand of these materials. Also, as labor has no direct environmental impact (or one that is negligible), it is also not included in an environmental LCI, at least not on the basis of man-hours.

To account for this difference, we have supplemented the data with processes like labor, and have attributed cost at the highest level in de LCI. For instance, instead of calculating the cost of input energy and materials using life cycle costing (LCC), we have instead used the market price of these inputs. In this sense, our study deviates from a true LCC. For each step in the production chain, the processing costs were calculated as follows:

$$CoP = \frac{\alpha \cdot I_{total} + \sum_{n=1}^{i} (cons_i \times \text{price}_i)}{T_{annual}} \quad (1)$$

where *CoP* is the cost of processing per unit of throughput, α is the capital recovery factor, I_{total} is the total investment expenditure for the processing tool, T_{annual} is the annual throughput of the processing facility, $cons_i$ refers to an annual amount of consumable input (material, labor, and energy inputs), price_i refers to the price per unit of $cons_i$. The capital recovery factor α is defined as:

$$\alpha = \frac{r}{1-(1+r)^{-D}} \quad (2)$$

where *r* is the depreciation rate and *D* is the depreciation period of the processing tool. The capital recovery factor expresses the annual depreciation and interest cost of the capital investment in the processing tool.

Cost data for process inputs was taken from a variety of sources. Equipment prices were taken from market surveys [27–31] for cell processing and from [18] for silicon and wafer production. For materials and energy we used data from literature, gathered average market prices, and included globally tradable products at international prices. The data gathered is summarized in Tables A7–A9 in the appendix.

2.4. Sensitivity and uncertainty analysis

The data we have gathered comes from a large variety of different sources, and as such can show large variety in both accuracy, quality and age. To investigate the sensitivity of the overall

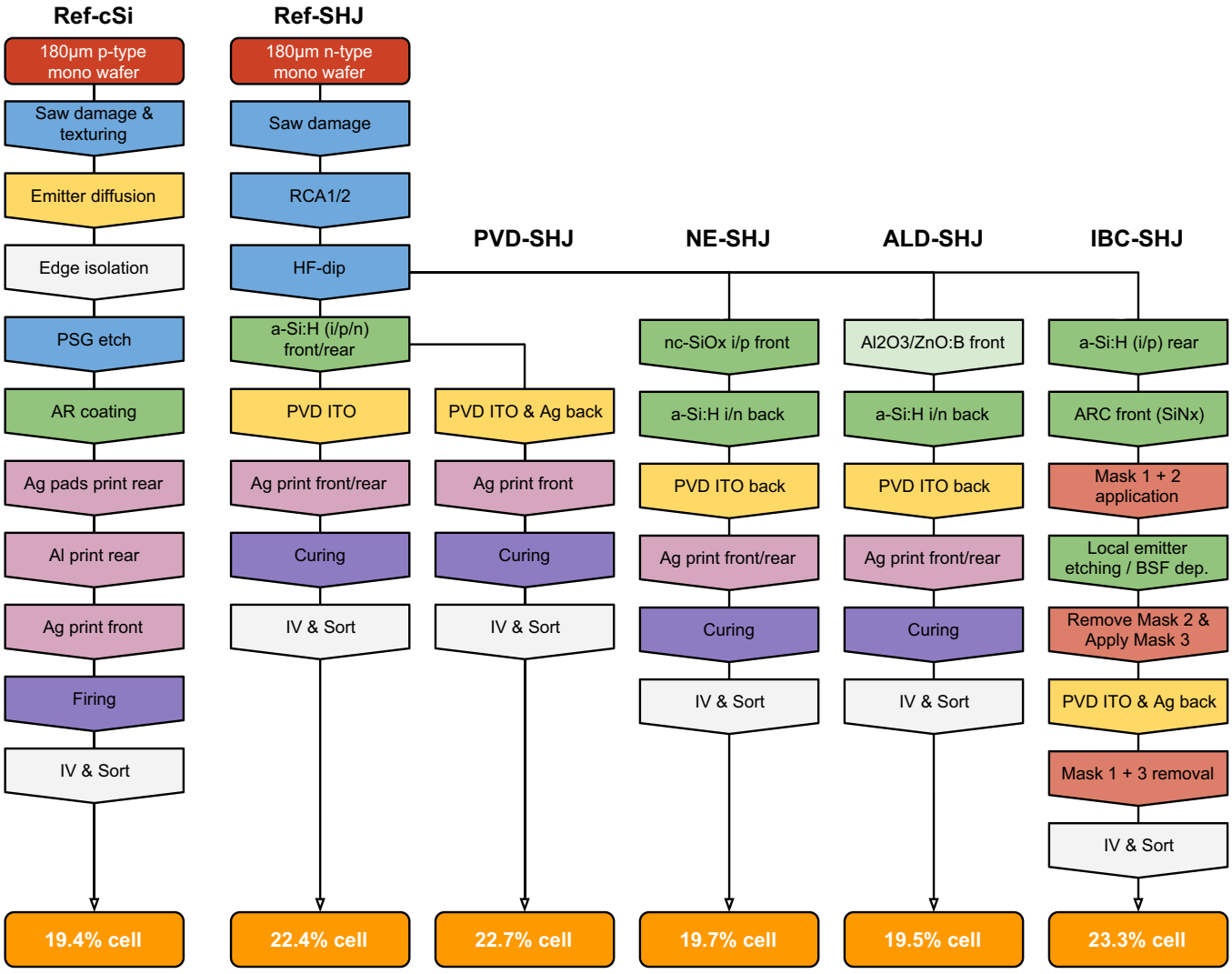

Fig. 7. Overview of cell processing steps for the different PV cell designs studied here. The process flow for the reference monocrystalline-silicon cell was based on [37].

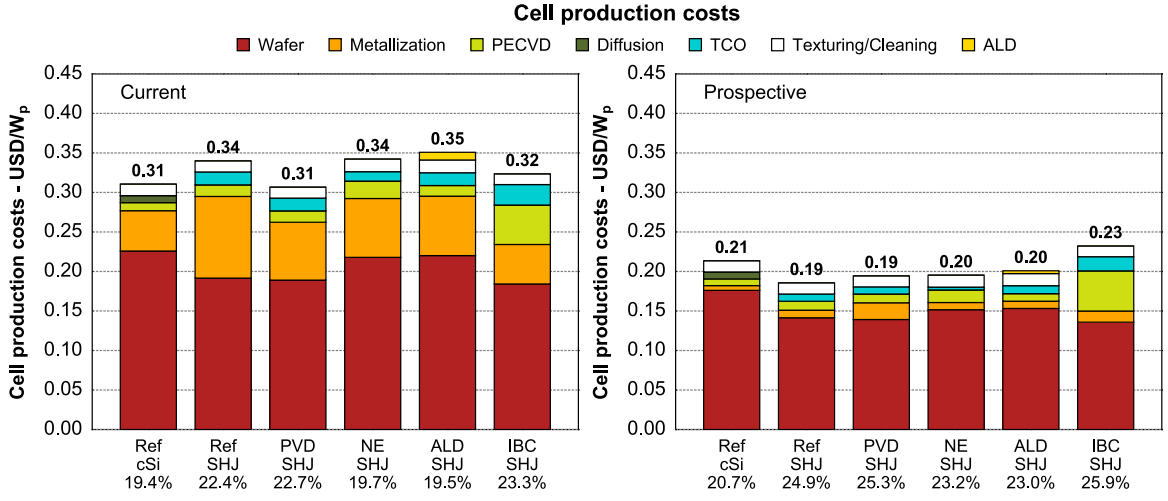

Fig. 8. Overview of cell production costs for the five silicon heterojunction designs and a conventional monocrystalline silicon device. Left: current production costs; Right: prospective production costs. The percentages below the labels indicate cell efficiencies.

result to variation in certain parameters, and to analyze the effect of uncertainty in the data on the overall result, we performed a sensitivity and an uncertainty analysis.

For the sensitivity analysis, we varied several parameters over a range defined by either historical data (for consumables, wafer price), or estimated ranges (cell/module efficiency). The resulting

Table 6
Main input parameters for wafer production.

	wafer thickness						
Input per m^2	**180**	**120**	**100**	**80**	**Unit**	**Unit cost (USD)**	**Source**
Cz silicon	0.74	0.54	0.49	0.38	kg		Own calculations based on [33]
Electricity	8.0	8.0	8.0	8.0	kWh		[33], assumed constant for varying wafer thickness
SiC fluid	1.2	0.7			L		[18,33]
- recycled	3.5	2.2			L		[33]
Cutting fluid			3.0	2.0	L		Assumption, cost from [18]
Steel saw wire	5.0	5.0			km	0.5	[34]
Diamond saw wire			83.0	83.0	m	0.125	Estimate based on [36]

recalculated overall results are plotted to show the overall result as a function of change in the studied parameter.

For the uncertainty analysis, we performed a Monte Carlo simulation. From the results and sensitivity analysis parameters were identified that have a large effect on the overall result and have considerable uncertainty. We generated 100,000 random samples of these parameters from log-normal distributions with means of the base values, and sigmas reflecting the uncertainty in each parameter. After that, the results were recalculated for each of the generated samples. The resulting data was presented as boxplots showing the variation in the overall result that was obtained. We opted to use log-normal (instead of normal) distributions as we assumed the parameters under investigation, such as module efficiency and prices, to be more constrained on one side of the mean, and to have a longer tail on the other side, e.g. the uncertainty was assumed to not be symmetrically distributed around the mean. The variance of the lognormal distribution was chosen so the 95th percentile of the distribution reflects the upper level of the uncertainty we want to investigate.

3. Production costs

3.1. Silicon, ingot and wafer production

The starting point for all of the devices analyzed in this study is a monocrystalline silicon wafer. Wafer production is generally an activity for dedicated wafer production companies, although supply-demand imbalances in the wafer production chain have resulted in an increased number of PV companies vertically integrating polysilicon, ingot and wafering in their activities [18]. Aside from more vertically integrated firms, the polysilicon production capacity has been expanded significantly since the price of polysilicon peaked in 2011. This has resulted in polysilicon prices dropping sharply, from around 80 USD/kg in 2011 to around 20 USD/kg from the end of 2012 until now (see Fig. 1).

The production chain for polysilicon, ingots and wafers is depicted in Fig. 5. From silica (SiO_2), which costs around 20 USD/tonne [32], metallurgical grade silicon (MG-Si) is produced by reducing the silicon-oxide with coke at high temperatures (1900 °C). As this process occurs in an electric-arc furnace, main inputs aside from the SiO_2 are electricity, and some form of carbon.

This MG-Si has a purity of about 98.5–99.5% [33], while much higher purity (99.99–99.9999%) is required in the solar and especially electronics industry. To achieve these higher purities, the MG-Si is processed into polysilicon, commonly using (hydro) chlorination in a Siemens reactor. A less common alternative is the Fluidized Bed Reactor (FBR), although due to technical challenges this process is not common [18], and is also more capital intensive compared to the Siemens process [34].

In the Czochralski (Cz) process, the polysilicon is “pulled” into monocrystalline silicon ingots, which are sawn into wafers with wire saws. In this process, silicon is lost as kerf loss, due to the abrasive sawing of the ingots into wafers. The silicon usage per wafer is reduced by decreasing wafer thickness and kerf losses. Current wafers are generally 180 μm thick [35], and sawing losses amount to 130 μm of silicon per wafer [18].

For material and energy requirements in polysilicon, ingot and wafer production, we used a life cycle inventory (LCI) from the ecoinvent database [33]. This database analyses the full life cycle of production of a 270 μm Cz wafer. The data from this inventory were updated to account for the different wafer thicknesses we investigated. Furthermore, as ecoinvent data does not accurately reflect the cost of capital expenditures, we based equipment and facility costs on Goodrich et al. [18], who studied the polysilicon-ingot-wafer production chain as a basis for cost roadmaps for various types of c-Si based PV modules.

By attributing costs to all the material and energy inputs from the LCI we calculated a cost structure for monocrystalline silicon wafers, from silica sand to wafer sawing. Table 5 shows the main input parameters for Cz ingot production. Fig. 6 shows the calculated cost structures for wafers of various thicknesses. The 100 and 80 μm wafers were assumed to be sawn with diamond wire saws (see Table 6).

3.2. Cell processing

The analyzed process flows are shown in Fig. 7. The basis for all designs studied is an 180 μm monocrystalline silicon wafer, n-type for the SHJ and p-type for the c-Si reference design. For simplicity, wafer costs are assumed equal for p-type and n-type wafers. The following section discuss the cell processing flow for each of the studied designs.

3.2.1. Conventional p-type c-Si cell

The p-type c-Si cell is assumed to be produced according to a standard process flow. Wafers are treated for saw damage and textured, prior to emitter diffusion in a diffusion furnace. After diffusion, a wet chemical treatment step is performed for edge isolation and phosphosilicate glass (PSG) removal. The silicon nitride (SiN_x) ARC is deposited with PECVD. Metallization is screen printed (Al with Ag soldering pads on the back, Ag grid on the front) and fired in a firing furnace at high temperature.

3.2.2. Reference SHJ cell

A reference case for SHJ cells was analyzed based on a conventional SHJ cell structure. The process flow for this Reference SHJ design (Ref-SHJ) is shown in Fig. 7, while the cell design is described in Table 1 and Fig. 3. The Ref-SHJ cell has a symmetric layout, with wafer, intrinsic a-Si:H, doped a-Si:H, ITO and metallization.

To treat the wafers for saw damage, texture it to achieve better light-trapping, and remove oxides from the surface of the wafers, the first process in the cell processing is at wet chemical

treatment. In our model, the wafers are treated with (1) Sodium hydroxide for saw damage removal, (2) A two step RCA cleaning procedure, and (3) a HF dip for oxide removal and texturing.

In terms of costs, this process main costs are consumables (the etchant solutions), capital expenditures (CapEx) and waste treatment. A survey on wet chemical treatment tools [27] shows average CapEx to be 293 ± 52 USD/(wafer/h), resulting in a wafer processing cost of 0.017 USD/wafer for capital investments, while total cost-of-ownership (CoO) including consumables is 0.075 USD per wafer. The etchants used in this process account for over 30% of these costs.

After wet chemical treatment, the electronic structure of the SHJ cell is applied by deposition of thin a-Si:H layers on both sides of the wafers. On one side, an a-Si:H (i) layer is deposited, followed by a p-type a-Si:H layer. On the other side, an i/n^+ a-Si:H stack is deposited. Main consumables are electricity, silane, hydrogen, and water. Because of the very thin layers applied (5 nm for the intrinsic layers, up to 20 nm for the doped layers) the material consumption is very low. As a result, most of the cost of this process step results from the capital expenditures for the processing tools. CapEx for PECVD was based on equipment costs for PECVD tools used for a-Si:H deposition in the preparation of thin film modules. A survey [30] showed large variation in the cost of these tools (ranging from 1489 to 5393 kUSD/(wafer/h), especially the older tools were found to have very high costs. PECVD tools for deposition of SiN_x ARC layers were found to have much lower costs, on average 882 USD/(wafer/h) [31], but as this process occurs at higher pressures, we assume these tools to be cheaper compared to those for a-Si:H deposition. We have selected the two most recent tools from the survey [30] to calculate PECVD costs for a-Si:H deposition, and found these to be 1676 USD/(wafer/h). Resulting processing costs were found to be 0.050 USD/wafer for capital expenses, or 0.078 USD/wafer including consumables and utilities.

PECVD is followed by the deposition of a TCO layer, in this case ITO, on both sides of the wafer. This transparent conductive oxide-layer is applied to improve lateral conduction in the device, while maintaining a high absorbance of light in the p/n region of the device. This deposition of ITO is commonly assumed to be expensive, as indium is a scarce and quite expensive material (750 USD/kg). According to our cost model however, this processing step is not as expensive as expected. The very thin layers deposited do not require much material (0.028 gram/wafer), and utilization factors in the sputtering tools are quite high (88%, resulting in ITO consumption of 0.032 gram per wafer). The cost of ITO target material was calculated to be about 0.85 USD/gram, although this is a rough estimation, and likely an overestimation, as we assume that commercial targets to approach raw materials prices (0.75 USD/gram). Capital costs for the sputtering tools we reviewed were found to be on average 1573 USD/(wafer/h) [28]. The total CoO of TCO deposition was found to be 0.087 USD/wafer, of which 0.027 USD/wafer (31%) was due to the consumption of ITO.

3.2.3. Silver-based metallization

A main cost factor in cell processing, as expected, was found to be the silver based metallization. As SHJ solar cells have to be processed at low temperatures (below 250 °C), there is a need for low-temperature silver paste. This paste is more expensive than conventional metallization paste, and more of it is needed to reach the required contact resistance values in the cells. We assume that the higher price of low temperature paste is mainly the result of a higher silver content in these pastes, but supply and demand dynamics possibly also play a role, as the market for low-temperature paste is much smaller to that of regular (high-temperature) paste.

Current silver paste cost were conservatively estimated at 820 USD/kg for high-temperature and 1060 USD/kg for low-temperature paste. Because of the lower conductivity of the cured low-temperature paste, we assume that double the amount of silver is required compared to high-temperature silver paste metallization. A metallization grid is therefore assumed to require 200 mg silver per side of the wafer, or 250 mg of paste, assuming 80% loading of the paste with silver. For the reference SHJ design, we assume that the application of a silver grid on both sides of the solar cell, thus the total paste requirement per cell is 0.5 grams. Total materials costs for metallization amount to 0.55 USD/wafer, or 0.10 USD/W_p. In current and past SHJ cell R&D many different metallization layouts have been studied for the backside of the cell, including silver screen printed grids, aluminium PVD back contact and silver PVD back contact. An aluminum backside would have the lowest material costs, but impacts the efficiency of SHJ cells severely as it is shown to result in a poor internal quantum efficiency in the infrared region of the spectrum without a more complex rear structure [38].

3.2.4. Silver PVD SHJ cell (PVD-SHJ)

The silver PVD SHJ cell (PVD-SHJ) is another design strongly based on the reference SHJ cell. Here, instead of a bifacial Ag grid, the backside contact is formed from PVD deposited silver. The cost of silver target material is lower compared to silver paste, resulting in a material cost decrease of 0.26 USD/wafer, to a total of 0.27 USD/wafer for metallization materials (0.059 USD/W_p). Here, we assumed that the thickness of the PVD deposited layer to be 0.2 μm [38], while the utilization rate of the PVD tool is assumed to be 74% [28], resulting in a silver consumption of 0.07 g/wafer for the rear side metallization. Capital costs do increase by 0.04 USD/wafer due to the PVD tool, but the resulting costs for metallization are still considerably lower at 0.33 USD/wafer compared to 0.55 USD/wafer for the bifacial silver grid.

3.2.5. Novel emitter SHJ cell

The novel emitter design is an SHJ design that focuses on replacing the scarce and expensive ITO with abundant materials, at the same time simplifying the processing sequence by cutting out on process, namely TCO deposition. The process flow for this design is shown in Fig. 7. As we can see from this figure, the basis of this design is very similar to the reference design. The changes occur however during the PECVD step. Instead of a p-doped a-Si:H layer, a transparent p-type conductive PECVD layer is deposited at the front side. The layer is deposited to function as both an emitter and a transparent conductive layer.

The replacement of the ITO layer on the front results in an increased requirement for PECVD. This does however not result in a strong decrease of throughput of the PECVD step as the p-layer is replaced by the combined layer and the main time-consuming factors are a result of creating and releasing the vacuum in the processing chambers, which is done once less. For the deposition of a total of 130 nm layer thickness, which is an increase in terms of total deposited layer thickness by a factor of 2.6, throughput drops with only about 4.5% compared to the reference design, based on throughput figures for a the selected PECVD tools mentioned in Section 3.2.2. This results in an increase of processing cost for PECVD by 0.025 USD/wafer to a total of 0.10 USD/wafer. The absence of the ITO deposition on the front however gives an advantage of 0.03 USD/wafer, largely due to increased throughput and an ITO consumption cost reduction of 0.013 USD/wafer.

3.2.6. ALD aluminum-oxide/zinc oxide SHJ cell

The ALD aluminum-oxide/zinc-oxide SHJ cell design (see Fig. 7) is an R&D design that tries to address two issues with conventional SHJ cells, namely (1) ITO replacement for more abundant ZnO and

(2) introduction of a thin-film deposition process that is less energy-intensive compared to PECVD and does not require operation at vacuum. The back-side of the cell is similar to that of the Reference SHJ and Novel Emitter SHJ design, with an i/n-stack of a-Si:H deposited with PECVD. On the front side, an Al_2O_3 passivation layer and ZnO window-layer are deposited with ALD and sputtering, respectively. Alternatively, this process could also involve MoO_3 as a high-workfunction hole-selective contact.

Average CapEx for the ALD tools surveyed [39] was found to be 796 USD/(wafer/h). As consumable consumption is low, the capital costs account for over 60% of the cost of processing a wafer with ALD. Another major factor is the cost of trimethylaluminum, which at 845 USD/kg accounts for over 20% of the cost of processing. Energy consumption in this atmospheric pressure process was found to be much lower compared to PECVD.

The relative cost of the PECVD deposition of the back-side i/n a-Si:H stack (25 nm total thickness) is quite high, as the throughput of the PECVD tool only increases by about 20% on average, while the capital related cost of processing only decreases by 11% compared to deposition of 50 nm of total a-Si:H layer thickness. As this cost advantage is minimal, the total cost of processing the ALD cell is slightly higher compared to that of the reference SHJ cell.

3.2.7. IBC-SHJ cell

The interdigitated back-contacted heterojunction (IBC-SHJ) cell is quite different from the reference design in terms of cell and module structure. The device has an assymetric structure, with interdigitated emitter and back-surface field and corresponding contacts. For this design we assume this interdigitated structure to be applied by using a masked PECVD deposition and etching process, based on a process described [40]. The process flow of this cell design is shown in Fig. 7, and detailed below.

The IBC-SHJ cell undergoes the same wet chemical treatment as the other designs, however, after this step the differences are pronounced. First with PECVD, on the front side of the cell a passivation layer (intrinsic a-Si:H) and SiN_x antireflective coating (ARC) are applied, while on the backside an a-Si:H emitter is applied. Then, a base mask is applied, followed by the mask for local plasma etching of the emitter and deposition of the a-Si:H backsurface-field (BSF). The BSF mask is removed and replaced with a second mask for TCO deposition and deposition of the evaporated silver back-contact. We have assumed that contact coverage at the rear side to be 80%, with a thickness of 0.4 micron, thus requiring 140 mg of silver target per wafer, assuming a 74% utilization rate in the sputtering tool.

We have assumed silver to be required for this IBC contact, as the reduced contact area would result in higher contact resistance when using aluminium.

The cost structure of production of this design is affected in three ways: (1) more processing steps are required, leading to a higher cost of capital, (2) replacement of the silver front grid with a silver PVD back-contact increases material costs for metallization, more silver is required for the back-contact, (3) the application and removal of masks increases handling, yield losses and material requirements.

Table 7
Overview of module component costs. Costs specified in USD/module relate to modules of standard size (1.65 m × 0.99 m).

Component	Cost	Unit	Source
Frame	13.5	USD/module	Market survey
Glass	5.50	USD/m^2	Market survey
Standard backsheet	5.04	USD/m^2	Market survey
SHJ backsheet with Al foil	7.00	USD/m^2	Own assumption
IBC backsheet with Cu foil	10.0	USD/m^2	[47]
EVA	1.85	USD/m^2	Market survey
J-Box	6.50	USD/module	[18]
Stringing/Tabbing	2.50	USD/module	[18]
Conductive adhesive	750	USD/kg	[47]

Table 8
Overview of difference in 60 cell module design and production between c-Si and SHJ modules.

Module element	c-Si	SHJ	IBC-SHJ
Stringing	Soldering tabber/ stringer	CA & tabber/ stringer[a]	CA & lamination[b]
Backsheet	Standard TPA	TPA with aluminium foil[c]	TP with structured Cu foil

[a] Cell stringing is assumed to be performed with a conventional tabber/stringer, but with conductive adhesive (CA) instead of regular solder.
[b] For IBC modules, we assume cell interconnection to be made during lamination, when conductive adhesive (CA) that was printed onto the structured foil is cured together with the EVA sandwich.
[c] SHJ modules are assumed to require a backsheet that is more resistant to moisture ingress. We assume this backsheet to be composed of a standard TPA backsheet with an additional aluminium foil layer.

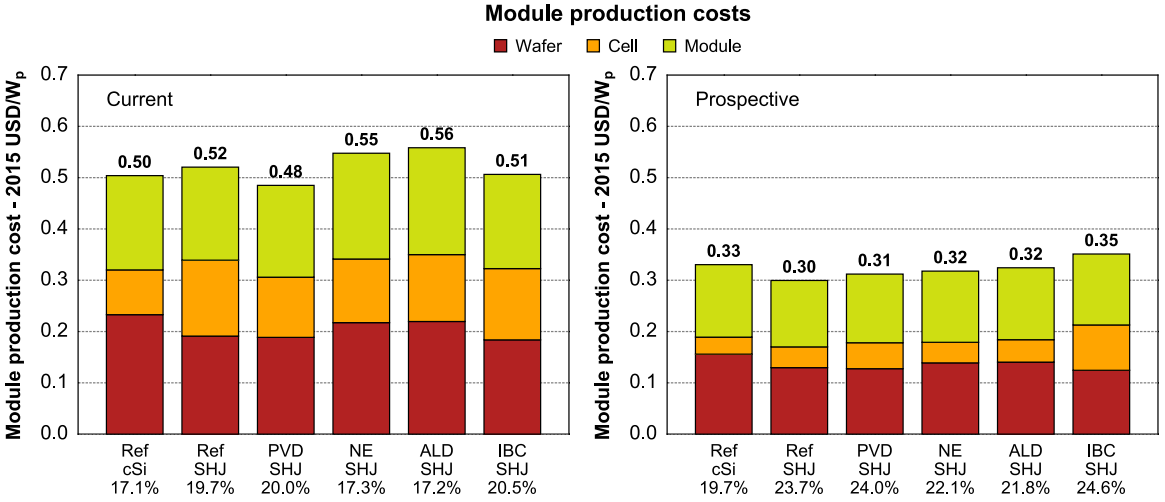

Fig. 9. Summary of total module cost for the monocrystalline silicon and SHJ designs. Totals are indicated in bold above the bars. A breakdown of cell costs is shown in Fig. 8. For a breakdown of the cost of module elements see Fig. 10. The percentages below the labels indicate module efficiencies.

Table 9
Effect of design changes on module production costs.

Improvement	Effect on production costs (USD/W_p)					
	Ref-cSi	**Ref-SHJ**	**PVD-SHJ**	**NE-SHJ**	**ALD-SHJ**	**IBC-SHJ**
Efficiency	−0.051	−0.060	−0.064	−0.088	−0.089	−0.071
Increased cell efficiency	−0.048	−0.057	−0.060	−0.083	−0.084	−0.067
Increased cell to module power ratio	−0.003	−0.003	−0.004	−0.005	−0.005	−0.004
Wafer	−0.056	−0.054	−0.042	−0.051	−0.054	−0.046
Metallization	−0.046	−0.093	−0.050	−0.064	−0.064	−0.034
Ag paste reduction	−0.018	−0.060	−0.029	−0.034	−0.034	0.000
Ag replacement with Cu	−0.029	−0.033	−0.020	−0.030	−0.030	−0.034
ITO replacement with ZnO	0.000	−0.010	−0.010	−0.008	−0.009	−0.010
Module Layout	−0.020	−0.025	−0.017	−0.028	−0.029	−0.017
Frame cost reduction	−0.020	−0.017	−0.017	−0.020	−0.020	−0.017
Bifacial module		−0.008		−0.009	−0.009	
Total	−0.174	−0.234	−0.182	−0.230	−0.235	−0.178

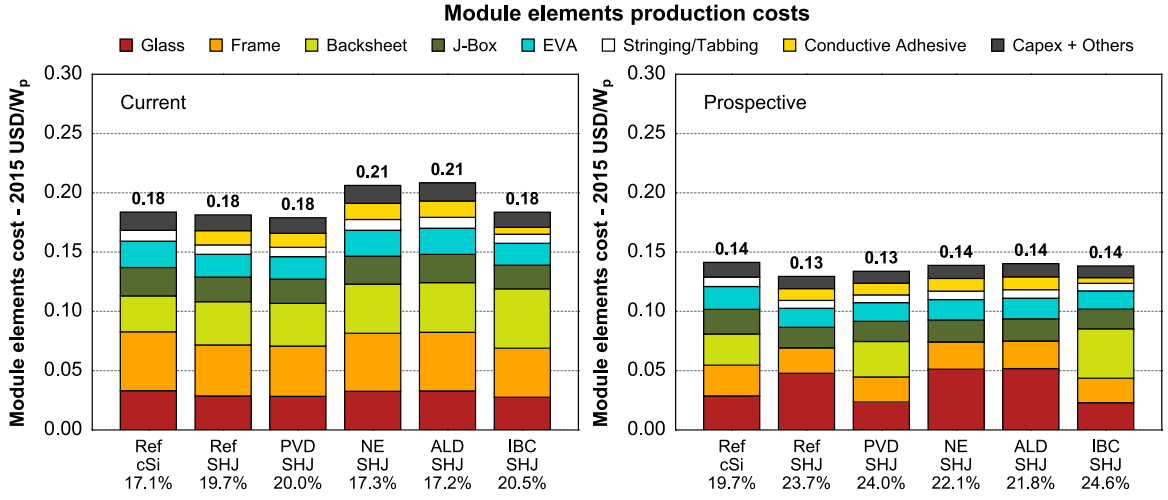

Fig. 10. Breakdown of the cost of module elements. Totals are indicated in bold above the bars. The percentages below the labels indicate module efficiencies.

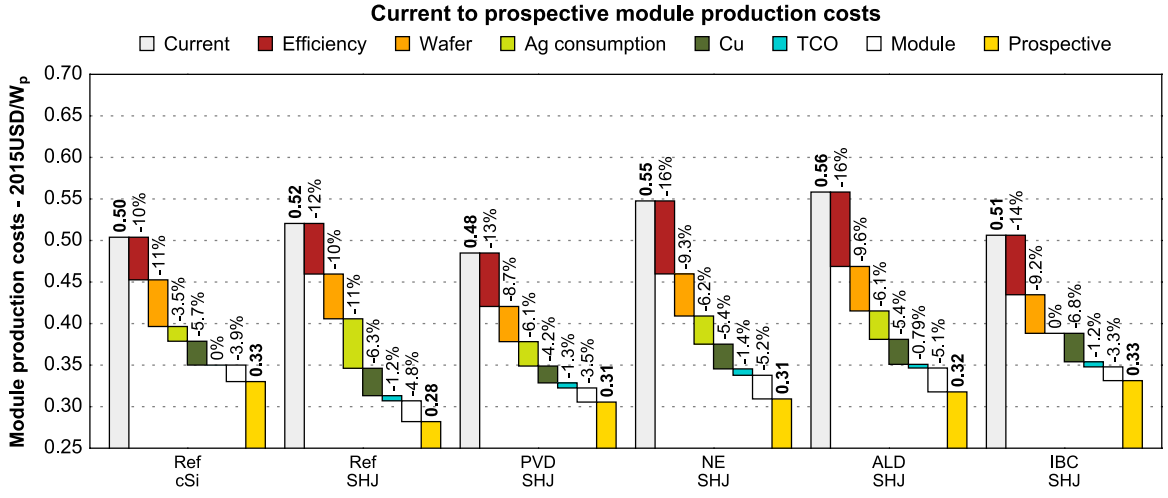

Fig. 11. Stepped bar chart showing the possible cost reductions achieved by changes in various parameters, from current to prospective designs.

To calculate the cost of producing the IBC structure, we have made several (rough) assumptions: (1) each process requiring a mask application or removal has a 10% lower throughput, (2) a mask application or removal step induces a 2.5% yield penalty, and (3) mask costs were estimated to be 0.05 USD/wafer.

The increased requirement of PECVD, coupled with the application and removal of masks, requires a three-step PECVD. This leads to a decreased throughput, and as a result, a strong increase in capital costs. Furthermore, material requirements are much higher, and yield losses increase due to the number of handling

steps when applying and removing the masks. The total cost of processing of PECVD therefore increases more than three-fold compared to the reference design, to 0.27 USD/wafer, of which 0.03 USD/wafer due to yield losses (compared to only 0.0011 USD/wafer for the reference SHJ design).

The replacement of the front-side silver grid made with low-temperature silver paste with an interdigitated PVD silver contact decreases the cost of metallization by 0.33 USD/wafer compared to the Ref-SHJ design. This is mainly the result of the substitution of low-temperature silver paste screen printed grid with a silver PVD metallization structure. Per watt-peak, metallization cost drop by 0.06 USD. Overall, CapEx costs increase by over 0.2 USD/wafer, but, due to the absence of low-temperature silver paste, consumable costs decrease by over 0.3 USD/wafer, resulting in processing costs that are 0.019 USD/wafer lower compared to the reference design.

3.3. Modules

For the current designs (except the IBC design), SHJ module production is quite similar to that of regular crystalline silicon modules, with the exception that the soldering step cannot be performed for SHJ cells, as this would lead to too high cell processing temperatures [19,41,42]. Therefore, the stringing and tabbing is performed with conductive adhesive (CA), which is cured during the module lamination step [41]. For the IBC-SHJ designs, the 1.8 grams/module of CA is printed as dot-contacts, while for the other SHJ designs, 3.6 grams/module of CA is applied on the busbars.

Before module production, cells are tested and sorted according to their IV-characteristics, so that they can be matched in 60-cell modules for an optimal power rating. Cells have to be handled to be layed up, tabbed and stringed and laminated into the module, in a sandwich of glass, backsheet and EVA. We reviewed CapEx for module production equipment [43–46] and found total costs for a module production line to be 4.8 ± 0.7 million USD for a line with a throughput of 60 modules/hr, resulting in a CapEx cost of 0.006–0.007 USD/W_p.

Conductive adhesive is more expensive than regular solder, mainly because silver is often used as a conductive material (as opposed to cheaper tin and lead). At the same time, the resistivity of conductive adhesive compared to regular solder is a concern [41]. For the performance stability of SHJ modules and protection against moisture related degradation, we assume the backsheet to be a combination of a standard Tedlar ® -Polyester-Polyamide (TPA) backsheet and an aluminium foil moisture barrier. Table 7 lists the costs of various module components assumed in this study. Prices for glass, frame, backsheet and ethyl-vinyl-acetate (EVA) where estimated based on average market prices.

The module design for the IBC-SHJ design is quite different. The interdigitated contacts mean that regular tabbing and stringing cannot be employed for cell interconnection. Rather, the cells are interconnected by glueing them with conductive adhesive to a backsheet/foil with prestructured copper contacts on it. The conductive adhesive is printed onto the foil in small dots. The EVA foil on the backside is patterned, to make holes at the points where the conductive adhesive is printed. The sandwich of glass, EVA, cells, patterned EVA, conductive adhesive, and backsheet/foil is laminated in one step in which the conductive adhesive is simultaneously cured. Table 8 summarizes the differences between the three module layouts (Table 9).

Fig. 10 shows a breakdown of module costs. Glass, backsheet and frame contribute most substantially to the overall module costs, while the addition of conductive adhesive results in a cost penalty of 0.007–0.014 USD/W_p for the SHJ designs. The structured backsheet for the IBC design increases the module cost by about 0.06 USD/W_p.

4. Prospective designs

The results for current designs indicate, as expected, main contributions for wafer and metallization to overall cell production cost. Other significant factors are PECVD and TCO sputtering while wet pretreatment of wafers contributes very little to overall production costs. In this paragraph we will detail, per processing step, a roadmap towards possible reduction of cell production costs. For this section we assume production in 2025.

4.1. Wafer costs

Logically, wafer prices are mainly influenced by two parameters: silicon usage per wafer, and silicon price per kg. Apart from a peak in the silicon price in 2008, silicon prices are relatively stable between 15 and 30 USD/kg (see Fig. 5). Cost reductions for silicon wafers therefore mainly focus on reducing wafer thickness and sawing losses. Goodrich et al. [18] project wafer prices to decrease significantly, due to these two cost reduction strategies, but also include the change from standard to diamond-wire saws, as this should increase throughput [35,48]. Diamond wire saws furthermore are more durable and do not require silicon-carbide slurry but work with a much cheaper cutting fluid based on water and surfactant [18].

Regular tabbing-and-stringing of cells into modules puts the solar cells under significant amounts of mechanical stress. With decreasing wafer thickness, this mechanical stress increases up to a point at which the cost reductions achieved by thinning the wafers is matched by the added cost of production yield losses. Therefore, we assume a minimum wafer thickness of 100 μm for all prospective modules.

In silicon production, a gradual shift from Siemens to Fluidized Bed Reactor (FBR) process that is already started is expected to continue, leading to a FBR market-share of just over 30% in 2025 [48]. FBR is currently a new technology and as discussed in Section 3.1, is quite complex. Cost reduction with this technology is therefore not currently expected [18]. Therefore, we modeled prospective silicon costs based on continued use of the Siemens process.

As shown in Fig. 6, even with conservative assumptions regarding silicon and wafer production, wafer cost can decrease substantially from the current modeled cost of 1.03 USD/wafer to 0.83 USD for diamond-wire sawn 100 μm wafers and 0.77 USD for 80 μm diamond-wire sawn wafers. However, it is not expected that module technology will be compatible with wafers below 100 μm by 2025, especially for monocrystalline cell based modules [48]. Therefore, we have based our prospective modules on wafers of 100 μm, for all cell designs. Although the low-temperature processing of SHJ cells is more compatible with thinner wafers than the higher temperature processing of standard c-Si cells, we have not assumed different wafer thicknesses to avoid bias in cost due to different wafer thicknesses.

4.2. Metallization

Cost reductions in solar cell metallization focus on two aspects: (1) reduction of material consumption and (2) substitution of high-cost metallization materials. Because of the high cost of silver-based metallization, the amount of silver used per cell has decreased, and is expected to continue decreasing for the coming years [35]. Although silver use per cell is constrained by minimum conductivity requirements [49], it is expected to decrease from 100 mg per cell in 2015 to about 40 mg/cell in 2025 [48]. This material use reduction alone results in significant cost reductions if application to all designs would be possible. For the conventional mono-crystalline cell, reduction from 100 to 40 mg/cell of

silver would drop metallization costs by 36%, or 0.02 USD/W_p. A reduction to 40 mg/cell of silver would actually mean that the Al-back paste would contribute the majority of metallization costs. However, as the Al paste is essential for the Al-BSF in the Ref-cSi design, the backside metallization of this design remains the same.

As the silver related metallization costs are much higher for the current SHJ designs (aside from the IBC design), the effect of this strong reduction in silver use per cell is very substantial. For the SHJ designs, metallization costs drop by 58% (Ref-SHJ), 49% (PVD-SHJ) and 45% (NE-SHJ and ALD-SHJ) or by 0.03 to 0.06 USD/W_p.

Further cost reductions can be obtained by replacing silver with copper. Copper has similar conductivity at only a fraction of the cost of silver. Currently, the cost of copper is less than 2% of the cost of silver. However, copper oxidizes much more easily compared to silver, and diffusion of copper into the silicon substrate is also an issue, as copper atoms diffusing into the silicon can negatively affect performance [50], through a variety of mechanisms [51]. Copper diffusion can be prevented by a nickel barrier layer, while oxidation is prohibited by covering the copper with a thin layer of silver applied with electroplating. Another approach to reduce copper oxidation is to dry/cure the applied metal contact lines in an inert (nitrogen) atmosphere [52]. Printed copper busbars that were printed on top of a SiN_x ARC and cured at low temperature in a <10 ppm oxygen atmosphere were shown to result in high module efficiencies, while subsequent thermal cycling and damp heat test showed no copper diffusion into the silicon [50]. Other recent results have furthermore demonstrated a newly developed copper paste that offers similarly low contact resistance compared to silver-based pastes, and can be cured at low temperature in "normal" atmosphere after screen printing [53]. However, line resistances were found to be much higher compared to both low temperature silver paste and high temperature silver paste [53].

In the area of copper metallization, copper electroplating is often mentioned as the prime candidate, as it has been shown to offer the possibility of high-efficiency, silver-free heterojunction solar cells, at a large cost-advantage compared to silver screen printed SHJ cells [54,55]. However, electroplated contacts require a multi-step process, consisting of screen-printing and curing a plating resist ink [18], plating different metal layers, and stripping the resist ink in a wet chemical tool. Despite this added complexity, the cost of plating is indeed significantly decreased compared to silver screen-printed contacts [55].

Although adoption of copper metallization in mass production of PV is not expected before 2018 [35], we have modelled our prospective designs with copper plated contacts, as we feel silver substitution is not only advisable for cost reductions, but also necessary, as silver is becoming an increasingly scarce material [56,57,49,58], so an upwards trend of the silver price is likely. The copper plated metallization assume a metal stack of nickel, as a seed layer and copper diffusion barrier, copper, as the main contact metal, and silver, as a capping layer which prevents oxidation of the copper. Electrolyte costs were modelled based on their composition, with the cost of plating equipment was taken from [55].

The cost reductions resulting from substitution of silver with copper result in additional cost savings of 0.01 USD/W_p for the Ref-cSi design, 0.03 USD/W_p for the Ref-SHJ design and 0.02 USD/W_p for the other SHJ designs.

4.3. TCO sputtering

Especially for SHJ solar cells, Indium-Tin-Oxide (ITO) is a commonly used TCO material. Because of the high cost and perceived scarcity of Indium, replacement of ITO with other materials is under investigation in many R&D projects. Zinc oxide, doped with boron or aluminium is a commonly named alternative [18]. Our results show that the deposition of ITO layers does not contribute much to the overall costs of cell and module production, as the amount of material used is very low. Still, we assume our prospective designs to be ITO-free, as there are concerns about the availability of indium [59,60] and ZnO targets were calculated to be slightly cheaper. Due to the higher resistance of ZnO compared to ITO, this replacement does however result in an efficiency penalty, due to an increased series resistance (R_s). Also, the workfunction of ZnO is sub-optimal for contacting a p-type a-Si:H layer. Aside from materials, TCO sputtering seems to be a mature process, with relatively low capital costs and high throughput.

4.4. Modules

Module design and materials have been largely the same for quite some time, and it is expected that the market shares of alternative module designs will remain limited up until 2025 [35,48]. Material use is expected to slightly decrease in the coming years, due to a step from 3.2 to 2 mm thick glass, decreasing EVA and backsheet thickness, and reduced aluminium usage in module frames [35]. For the aluminium frame we assume that the cost is reduced proportionally to the mass decrease shown in [35]. For the other materials, accurate data could not be found. Increased light transmission and trapping for the modules results in a slight increase of cell-to-module power ratio [35].

On the other hand, because of the high price of silver, the silver content of conductive adhesive will likely decrease further. Another development is the increasing attention for frameless and/or bifacial modules. In these modules, the backsheet is replaced with another pane of glass, and, possibly, the frame is also omitted.

The Ref-SHJ, NE-SHJ and ALD-SHJ designs in our prospective study are bifacial by design, thus, their prospective module layouts are assumed to be bifacial, replacing the backsheet with a pane of glass. For the Ref-cSi design and the other SHJ designs, we assume a standard module layout, with a backsheet. We assume all modules to have an aluminium frame, which is, as discussed above, decreased in weight and cost.

5. Current and prospective cell and module production costs

Cell production costs (in USD/W_p) are shown in Fig. 8. As expected, a main contributor to cell production costs is the wafer, for all designs. The SHJ designs have cell production costs ranging from 0.31 to 0.35 USD/W_p, while the cell production cost for the c-Si cell was found to be 0.31 USD/W_p. The IBC design benefits strongly from its high efficiency and substitution of silver paste with PVD silver, which offsets the cost penalties for lower yield and throughput, while the bifacial Ref-SHJ cell shows a strong cost-penalty for requiring a large amount of low-temperature silver paste. The novel emitter and ALD SHJ designs are affected by their lower efficiency, and thus have higher production costs compared to the reference design. The PVD-SHJ design has the lowest cost of the SHJ designs, as it benefits from high efficiency and substitution of low-temperature silver paste.

Comparing the Ref-cSi cell with both the Ref-SHJ and PVD-SHJ designs shows that the choice of metallization layout likely determines the competitiveness of SHJ technology. There is a strong cost penalty for using silver paste on both sides of the SHJ cell, that cannot be offset by the increase in efficiency.

When intercomparing the SHJ designs, we see that the replacement of the front ITO in the NE-SHJ design does not result in a cost reduction compared to the Ref-SHJ design, as there is a

significant assumed efficiency penalty for this novel SHJ design. For the ALD-SHJ design, this effect is also shown.

As indium is a relatively expensive material, the effect of replacing the ITO layer was expected to be larger. However, the LCA model [13] already showed that only very small amounts of indium are required as the layer thickness is very small. For two 80 nm layers of ITO, slightly over 0.03 grams of ITO was calculated to be required per cell (based on typical utilization rates, density of ITO, and the volume of the layer). The increased requirement for PECVD in the novel emitter design slightly decreases the advantage obtained by having no sputtered TCO layer, as the increased a-Si layer thickness leads to a slightly decreased throughput, and thus an increased cost of processing (*CoP*, see Eq. (1)). The main determinant for higher production costs of the NE-SHJ design is however the decreased efficiency compared to the Ref-SHJ design.

5.1. Module costs

Fig. 9 shows the costs of complete PV modules based on the designs studied, while Fig. 10 shows the cost of the module materials. The requirement of conductive adhesive results in a small cost penalty for SHJ modules, while the structured back foil required for the IBC-SHJ design results in a larger cost increase for this particular module. These added costs compared to conventional modules are not completely be balanced by the increased module efficiencies. Especially for the NE-SHJ and ALD-SHJ designs, the relative increase in efficiency is to small to offset added costs of cells and module components. For the Ref-SHJ design, the expensive metallization layout results in higher module costs.

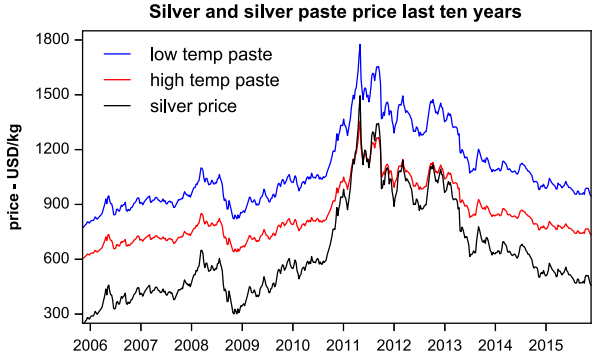

Fig. 12. Silver price, and estimated high- and low-temperature silver paste price from October 2005 to October 2015. Silver price data: [18,63].

As a result, only the PVD-SHJ design has lower total module costs of 0.48 USD/W_p compared to 0.50 USD/W_p for the Ref-cSi module. The other SHJ designs have cost ranging from 0.51 for the IBC-SHJ design, to 0.56 USD/W_p for the ALD-SHJ design.

For the SHJ designs, the wafer and module contribute about 36–39% and 35–38% of the overall costs, respectively. Cell processing contributes 23–24%, for the designs with an PVD Ag back contact (PVD-, NE- and ALD-SHJ), 27% for the IBC-SHJ module, and 28% for the Ref-SHJ module. For the reference c-Si module, due to lower efficiency and cheaper cell processing, the contribution of wafer and module cost (46% and 37%) is much larger compared to that of cell processing (17%).

5.2. From current to prospective production costs

In Section 4 we identified several developments and pathways towards reduction of PV production costs. To summarize, these were: (1) Increased cell and module efficiency for all designs (2) Decreased cost of wafers due to higher silicon utilization (thin wafers, less kerf loss) (3) Reduction of silver usage per cell followed by (4) Substitution of silver with copper (5) Replacement of ITO with ZnO, and (6) Slight changes to the module frame.

Fig. 11 shows the effect of these changes on the five module designs studied here. Major cost reductions can be obtained by improved cell efficiency and lower wafer production costs. The increased efficiency of the prospective SHJ designs leads to a cost decrease of 12–16%, while this figure is 9.6% for the reference c-Si design. Higher silicon utilization due to thinner wafers, produced with less silicon kerf losses, allow for a reduction in cost of 9–10% for the SHJ designs (11% for c-Si). The reduction of silver consumption projected by the International Technology Roadmap for Photovoltaics [48], of about 60% in 2025, would allow for a cost reduction of 11% for the silver-heavy Ref-SHJ designs, and 6% for the remaining SHJ designs with screen printed Ag grids. Substitution of silver with copper-based metallization would allow for a further decrease of 4–7%. Silver use reduction (−4%) and substitution (−6%) would not decrease the production costs of the conventional c-Si module as much, as the contribution of metallization cost to overall costs is much lower (see Fig. 8). Replacement of TCO would allow for cost reduction of around 1%, while reduction in the amount of aluminium used for the module frame and a switch to bifacial modules where possible, would allow for a further cost reduction of 3–5% for all designs.

Combined, these developments result in a significant expected drop in cell production costs and total module costs. Cell processing costs drop by 62% for the Ref-cSi design, 73% for the Ref-SHJ

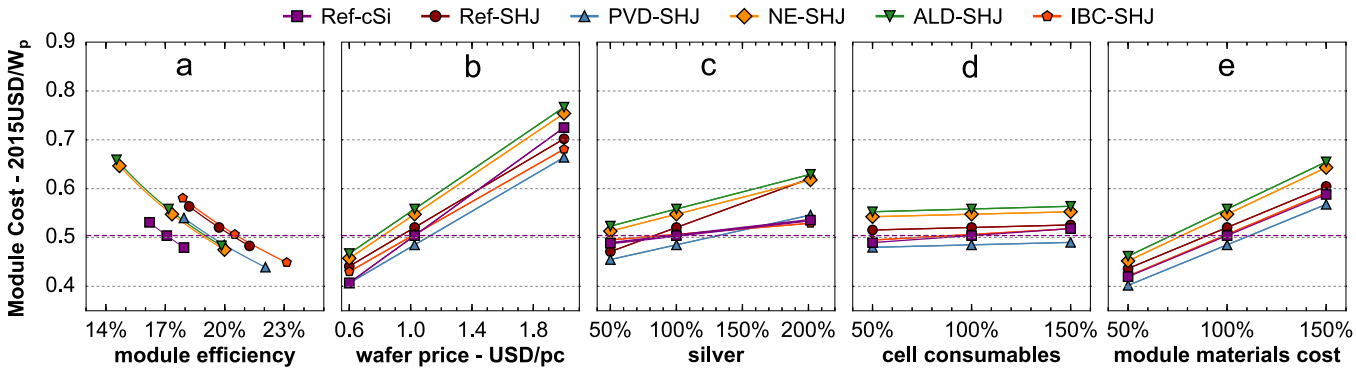

Fig. 13. Results of the sensitivity analysis. The graphs indicate the change in overall results as a function of change in module efficiency, wafer price, silver price/consumption and consumable price/consumption. The colored markers indicate the minimum, base and maximum results for each of the studied designs. Module efficiency was varied over a range we estimated. Wafer price and silver price were varied over a range reflecting these parameters' historical (5 year) variation. Consumable prices were varied over a range we assumed to account for most variation found on the market. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.).

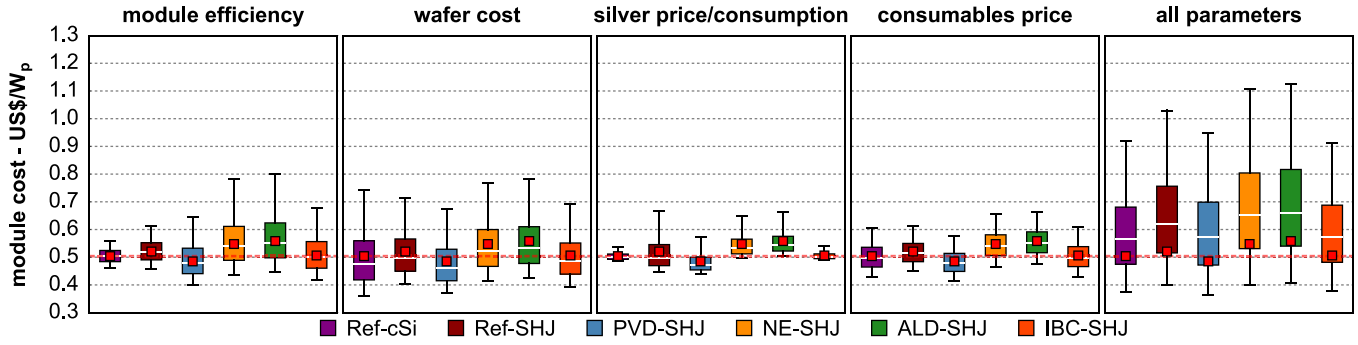

Fig. 14. Results of the Monte Carlo uncertainty analysis. The box plots indicate the range in overall results obtained when varying efficiency, wafer price, silver price/consumption and consumable price/consumption The red squares and white lines indicate mean and median values respectively, while the boxes indicate 25th and 75th percentiles, and the whiskers indicate minimum and maximum values. The dashed red line indicates the main result for the Ref-cSi design. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

Table 10
Overview of parameter ranges studied in the sensitivity analysis (min-max range) and Monte Carlo simulation (σ).

Parameter		Ref c-Si	Ref-SHJ	PVD-SHJ	NE-SHJ	ALD-SHJ	IBC-SHJ
Module efficiency	base	17.1%	19.7%	20.0%	17.3%	17.2%	20.5%
	min	16.2%	18.2%	17.9%	14.7%	14.5%	17.9%
	max	17.9%	21.2%	22.0%	20.0%	19.8%	23.1%
	σ[a]	0.4%	0.8%	1.0%	1.4%	1.3%	1.3%
Wafer price	base	1.03	1.03	1.03	1.03	1.03	1.03
	min	0.80	0.80	0.80	0.80	0.80	0.80
	max	2.00	2.00	2.00	2.00	2.00	2.00
	σ	0.128	0.255	0.255	0.255	0.255	0.255
ag paste price/consumption	base	100%	100%	100%	100%	100%	100%
	min	50%	50%	50%	50%	50%	50%
	max	200%	200%	200%	200%	200%	200%
	σ	0.128	0.255	0.255	0.255	0.255	0.255
Consumable price/consumption	base	100%	100%	100%	100%	100%	100%
	min	50%	50%	50%	50%	50%	50%
	max	150%	150%	150%	150%	150%	150%
	σ	0.255	0.255	0.255	0.255	0.255	0.255

[a] The sigma (standard deviation) was calculated assuming the respective min-max ranges to be the lower and upper bounds of the 95% confidence interval.

design, 67–68% for the ALD-SHJ and NE-SHJ designs, 57% for the PVD-SHJ design, and 36% for the IBC-SHJ design. Total module costs drop by 34% for the c-Si module, 31% for the IBC-SHJ module and, 36–42%, for the other SHJ modules. As Figs. 8 and 9 show, they would thus allow for cell production cost of 0.19–0.23 USD/W_p and 0.21 USD/W_p for SHJ and c-Si cells respectively, and 0.30–0.35 USD/W_p and 0.33 USD/W_p for SHJ and c-Si modules, respectively.

The IBC module shows the least potential for cost reduction as its' prospective costs are hampered by the requirement for the structured backsheet, the high capex costs, and the high yield and throughput losses incurred by the complex processing sequence.

6. Sensitivity and uncertainty

The cell and module production costs shown above rely heavily on a few major parameters: (1) Uncertainty in cell and thus module efficiency; (2) Historical variation in wafer cost; (3) Variation in silver paste price and uncertainty in silver consumption per cell, and (4) Uncertainty in prices of consumables. We performed a sensitivity and uncertainty analysis, to show the sensitivity of the overall results to changes in these parameters and to assess the effect of uncertainty in these parameters on the overall result. To analyze the sensitivity of the overall results to these parameters, we varied the parameters and plotted the resulting module costs in Fig. 13. For the uncertainty analysis, we performed a Monte Carlo simulation: random samples for each parameter were generated from a log-normal distribution, and the overall module cost was recalculated with these random samples. For instance, we generated 100,000 module efficiencies randomly from a log-normal distribution and recalculated module costs with these 100,000 samples. The resulting ranges of results are represented as box plots in Fig. 14 showing the distribution of obtained module costs.

Table 10 shows the parameters we investigated, the ranges over which we varied them, and the standard deviation we used to generate the random samples for the Monte Carlo simulations. The results of the sensitivity and uncertainty analysis are shown in Figs. 13 and 14 respectively.

6.1. Cell and module efficiency

As the novel SHJ designs studied here are still under development, accurate measurements of cell efficiency in mass production or even pilot production are not yet available. Furthermore, as

shown in Section 5.2 and Fig. 11, a large fraction of prospective cost reductions relies on an assumed increase in cell and module efficiency. Recent development of varying designs show significant variation in SHJ cell efficiency [19].

We assigned an efficiency range to each of the studied designs, assuming that the efficiency of the Ref-cSi design has the smallest uncertainty, being the most established cell design. For the SHJ designs, the range in efficiencies analyzed is larger, especially for the conceptual NE-SHJ and ALD-SHJ designs. The ranges studied are shown in Table 10. These ranges were estimated roughly, based on the deviation of the designs' layout and processing cycle from that of the Ref-SHJ design.

As shown in Fig. 13(a), module cost is quite sensitive to changes in module efficiency. When we varied cell efficiency over the ranges described in Table 10, costs change with a factor of the inverse of the relative efficiency change. The figure clearly shows that the Ref-cSi design has a pronounced processing cost advantage, that is offset only by strong efficiency increases in the PVD-SHJ and IBC-SHJ designs. The other SHJ designs need further efficiency improvements to approach Ref-cSi module costs. At similar efficiency, the SHJ would be more expensive compared to the c-Si module, due to the high cell and for the IBC design also module costs.

6.2. Wafer cost

Wafer prices are strongly linked to polysilicon prices, which have shown to be quite volatile. Current (June 2015) spot prices for wafers are about 1.01 USD/wafer, with polysilicon prices at around 15.7 USD/kg [61]. After many silicon producers shutting down the last 1.5 years due to an oversupply, prices were estimated to stabilize and rise slightly to a price of about 20–25 USD/kg [62]. More recently, polysilicon capacity was increased, leading to the possibility of another polysilicon oversupply situation with further price decreases. Polysilicon price is thus quite uncertain. Taking into account the price range of polysilicon for the last 5 years and possible further price decreases, we investigated the effect on the overall results of a wafer price in the range of 0.60 USD/wafer to 2.0 USD/wafer.

Fig. 13(b) shows that all designs are quite sensitive to variation in wafer cost. The effect of changes in wafer cost is similar for all devices, although the effect is more pronounced as the module efficiency decreases, as the wafer cost contributes more to the overall costs at lower efficiencies. This is especially apparent in the results for the Ref-cSi module, and to a lesser degree for the ALD-SHJ and NE-SHJ modules.

6.3. Silver paste price and consumption

Another strong contributor to overall cell manufacturing cost is the price of silver paste used for metallization. As shown in Fig. 12, silver prices are quite volatile, with prices ranging from about 500 USD/kg to over 1700 USD/kg over the last five years, with a current (Oct 2015) price of about 520 USD/kg. This silver price variation could account for very large increases in the cost of silver paste, to almost 1500 and 2000 USD/kg for high and low temperature paste, respectively.

Because of the requirement for relatively large amounts of silver in low-temperature paste, the SHJ designs are quite sensitive to changes in paste price or paste consumption per cell, especially the bifacial Ref-SHJ design. A doubling of the paste price would raise the production costs of this designs by up to 20%. The effect is not as strong for the c-Si design, as this design is based on cheaper, high-temperature paste.

6.4. Other consumable prices

Price variation can of course occur not only for silver, but also for all other material consumables that are required to produce the solar cells and modules. Therefore, we studied the effect of variation in the prices of cell consumables other than silver paste and wafers, and of module materials on the overall results. As seen in Fig. 13(d), the effect of changes in cell consumable prices is limited, as these consumables only account for around 2–5% of SHJ module prices and 9% of the Ref-cSi module. The results are however very sensitive to changes in the cost of module materials (see Fig. 13(e)), as they contribute around 30–40% of total module cost.

6.5. Monte Carlo uncertainty

The results of the Monte Carlo simulation to assess the effect of uncertainty in the data is shown in Fig. 14. This figure shows the distribution of relative cost of the SHJ designs compared to the Ref-cSi design. This figure shows that especially uncertainty in module efficiencies can alter the results (absolute and relative) significantly. Uncertainty in the cost of wafers, silver, and other consumables also has a pronounced effect on module prices (as shown also in Fig. 13(b)–(e)) but changes in these parameters would likely affect all designs similarly and thus not significantly changes the relative results.

7. Discussion and conclusions

The main aim of this study is to perform a bottom-up analysis of the relative cost of different silicon heterojunction (SHJ) based PV modules, and to compare current and prospective costs of these modules with those of a conventional monocrystalline silicon module. The aim is to develop a methodology that allows for ex-ante screening of R&D cell concepts. We performed a life cycle costing analysis to analyze in detail the cost structure of the production of PV modules, and found current SHJ modules to be comparable in price compared to conventional monocrystalline silicon modules, but cost penalties incurred by using more expensive materials need high efficiencies to be offset. Thus, especially designs that minimize the use of low-temperature silver paste benefit from the efficiency advantage of heterojunction technology.

The life cycle costing (LCC) method shows its' usefulness in determining the contribution of each process and material input to the overall production cost of different cell and module designs. Our research has confirmed that for all designs investigated wafer and metallization contribute the majority of overall cell production costs, while for complete modules, the module materials are also a very significant cost factor. Reductions in wafer thickness, silver paste usage, or substitution of silver with copper-based metallization allows for significant cost reductions. The strong effect of module efficiency on module price (USD/W_p) however shows that changes in cell and module design that have a negative effect on module efficiency will likely result in a relative cost increase. Furthermore, as Fig. 13 (a) shows, the efficiency advantage of the studied SHJ designs is the main reason for there lower production costs (in terms of USD/W_p). This indicates that: (a) the uncertainty in cell and module efficiency for the SHJ designs results in significant uncertainty of the overall result (see Figs. 13 and 14), (b) changes in cell processing that decrease cell efficiency are likely to result in cost increases, even if they reduce cell processing costs, (c) accurate cost calculations for SHJ cell concepts should preferably rely on cell efficiency data from gathered from (pilot) production lines.

7.1. Wafer cost

To calculate the wafer production cost, we performed an LCC analysis of wafer production from silica to sawn wafers. Our model results for current wafers (1.03 USD/pc) results in slightly higher costs compared to the current wafer spot price (1.01 USD/pc) [61]. This likely is the result of the fact that the life-cycle data on silicon production we used for our calculations is already some years old (from 2007), although we have updated this as much as possible, as progress has been made especially in reducing the energy budget of silicon production. A different issue with our model is that we have used a single cost model for the wafer used, e.g. we have not distinguished between *n*-type and *p*-type wafers. It is sometimes assumed that *n*-type wafers are likely to be more expensive compared to *p*-type wafers because of lower yields, more complex processing and added capital expenses, however this has been disputed [18].

7.2. Metallization

In PV industry and research, it is common knowledge that metallization is a main contributor to PV module costs. R&D on alternative metallization schemes is therefore a very active field of research. The amount of silver used per wafer has already dropped significantly [35], a trend which is expected to continue. Our results indicate that a projected reduction in silver use per cell [35] could decrease the costs of the silver-based SHJ modules studied here by about 6% for most designs, but up to 11% for a design with high silver consumption. As conventional c-Si cells use cheaper silver paste, containing less silver, this cost reduction potential is smaller (−4%) for this technology.

Aside from material use reduction, replacement of silver with copper is also being heavily researched, mainly through research on copper-plating. Copper offers similar conductivity, at only a fraction (~2%) of the cost. Furthermore, the supply of copper is less constrained, although not impervious to price volatility. Our results show that silver substitution could decrease module cost by an additional 4–7% for SHJ modules, or 6% for c-Si modules. In our prospective designs, the contribution of metallization is already low, as we assume that paste consumption per wafer to substantially decrease.

The adoption of copper in the manufacturing process is however not without issues: copper rapidly oxidizes during thermal curing, and can diffuse into the silicon cell substrate [35,53,52]. Recent results have however shown that contact curing can be performed with minimal oxidation in inert or low-oxygen curing atmospheres [52,50], or in normal atmospheres using a specially developed paste [53]. Furthermore, the ITO layer applied in SHJ solar cells is stated to be an effective barrier to metal diffusion [64]. Especially copper-plated contacts however, in conjunction with a nickel seed layer and silver capping layer, show prospects for high efficiency SHJ solar cells [54].

An issue with our current model for metallization costs is the cost-structure of metallization pastes. There is limited information on the cost of these pastes, but the available data shows that these pastes are much more expensive than pure silver. This indicates that a significant fraction of metallization paste cost is non-silver related (460 and 580 USD/kg for high- and low-temperature paste). For aluminium pastes, this does not seem to be the case, as these pastes are much cheaper (~50 USD/kg). It does however seem to indicate that the cost in front-side metallization paste (especially low-temperature) cannot only be reduced by reducing the silver content or replacing silver with another metal. Alternative forms of metallization, such as SmartWire Connection Technology [65], inkjet or stencil printing or electroplating could possibly offer further metallization cost reductions.

7.3. ITO replacement

From a cost perspective, replacement of ITO has very limited benefits, as the amount of indium needed for the thin transparent conductive oxides is very low. Alternative TCO's that are cheaper but less conductive, are likelier to increase the module cost due to decreased cell efficiency. As one of the options, we have also modelled replacement of ITO with ZnO, which offers a very modest cost decrease.

At current price levels (June 2015, 750 USD/kg), ITO contributes about 0.8–1.8% of cell costs and 0.5–1.1% of total module costs. As we have possibly overestimated the cost of ITO target material (see Section 3.2.2), this contribution could be smaller. Thus, from a cost perspective, ITO replacement does not seem to be that important. At a 100% price increase for ITO, the contribution increases slightly to 1.0–2.2% of module costs. The development of alternative TCOs should however still be researched, as the availability of indium could become a concern [59,60].

7.4. Module design and materials

Our results indicate that module materials already contribute a large fraction of overall module cost, and will likely contribute the majority of module costs as wafer and cell production become cheaper. Cost reduction possibilities in module design are likely limited, as the production of the materials used is already very mature, and there is thus limited possibility for technological learning. For current modules, main costs are glass, frame and backsheet. Prospective glass-glass modules can be somewhat cheaper compared to modules with an aluminium frame, because of the replacement of the backsheet with a sheet of glass. The cost of the glass on the backside of the prospective modules is likely overestimated, as lower quality glass can be applied here compared to the front-side. This could significantly lower the price of the backside of the module. Furthermore, the costs calculated here are based on monofacial efficiencies, and thus do not reflect the additional energy yield than can be obtained from bifacial PV modules.

7.5. Concluding remarks

Our results show that silicon heterojunction (SHJ) technology offers the potential for cost reductions in PV manufacturing compared to conventional crystalline silicon solar cells and modules, especially for prospective PV modules. Heterojunction module production costs were found to range from 0.48 to 0.56 USD/W_p, compared to 0.50 USD/W_p for a conventional monocrystalline silicon module. Heterojunction modules incur a strong cost penalty because of the requirement for low-temperature silver paste. High-efficiency SHJ designs that minimize the use of this paste can be competitive with standard crystalline silicon PV modules. As the designs studied are conceptual, the validity of the results will strongly benefit from more accurate determination of the efficiency of SHJ cells and modules from large-scale production. Variation of material prices can also have a large influence on the cost of SHJ modules, but these variations will likely affect all designs similarly and thus not alter the relative results.

Our results confirm that the choice of metallization has a substantial impact on the cost of SHJ modules compared to conventional crystalline silicon modules. This is mainly due to the high cost of low-temperature paste needed for SHJ cell processing, and the increased amount of paste required due to its lower as-cured conductivity. This results in higher cell costs for SHJ designs (USD/cell), that is offset partly by the high efficiency of heterojunction technology.

Our prospective analysis indicates that a reduction in paste consumption and replacement of silver with copper paste could alleviate this problem, e.g., the cost-advantage of SHJ cells becomes less dependent on the efficiency advantage. However, these results are based on the assumption that progress in reduction of silver consumption is also applicable to SHJ cells. A more promising approach seems to be the replacement of screen printed silver grids with copper-electroplated contact, minimizing the amount of silver used in SHJ cells.

For all studied prospective modules, the module materials contribute significantly more to the overall module cost than they do now.

Interdigitated back-contacted (IBC) design are often mentioned as a promising low-cost (future) module technology. Our results however show that for now, the requirements for this technology during cell processing and module production cannot be completely offset by the large efficiency advantage obtained through the improved cell structure.

As the prospective cost reductions that we have modelled are very dependent on reductions and eventual elimination of silver use in SHJ cells, further research should keep addressing these issues, by establishing a metallization process based on copper that is compatible with industrial scale production without adding complexity to the production process. Furthermore, increasing attention should go towards reducing the cost of module elements.

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Appendix A. Input data

Table Tables A1–A9.

Table A1
Equipment cost. Variability refers to the standard error of the mean.

					at 3600 wafers/hr		
Tool	**Avg Price** (kUSD)	**Variability** (kUSD)	**Avg Throughput** (wafers/hr)	**Variability** (wafers/hr)	**Price** (kUSD)	**Variability** (kUSD)	**Source**
Diffusion Furnace	1915	287	2812	493	2707	251	[66]
SiNx PECVD reactor	1496	95	1760	157	3174	240	[31]
a-Si:H PECVD reactor	7325	5317	1763	588	5362	79	[30]
Spatial ALD	1948	477	2517	332	2866	263	[39]
Sputtering tool	6060	825	4059	456	5662	851	[28]
Screen printer	353	49	1669	176	732	64	[67]
Plating tool	1617	383	3900	900	1128	323	[55]
Tabber/stringer	495	142	1044	236	1832	420	[46]
Cell tester	156	14	2300	313	302	38	[43]
Cell sorter	737	132	2401	209	1055	134	[43]
Layup machine	212	8	2211	78	397	15	[44]
Laminator	446	34	1592	91	1208	100	[45]

Table A2
Texturing/cleaning – Main input parameters.

Input	**Unit**	**Ref-cSi**	**Ref-SHJ**	**PVD-SHJ**	**NE-SHJ**	**ALD-SHJ**	**IBC-SHJ**
Hydrogen fluoride	g/wafer		0.918	0.918	0.918	0.918	0.918
Sodium hydroxide	g/wafer	3.820					
Hydrogen peroxide	g/wafer		0.870	0.870	0.870	0.870	0.870
Hydrochloric acid	g/wafer	1.110	0.581	0.581	0.581	0.581	0.581
Ammonia	g/wafer	0.164	0.212	0.212	0.212	0.212	0.212
Ethanol	g/wafer	0.156					
Isopropanol	g/wafer	1.920	1.920	1.920	1.920	1.920	1.920
Solvents	g/wafer	0.034					
Acetic acid	g/wafer	0.068					
Nitric acid	g/wafer	0.649					
Calcium chloride	g/wafer						
Sodium silicate	g/wafer						
Potassium hydroxide	g/wafer						
Electricity	kWh/wafer	0.031	0.066	0.066	0.066	0.066	0.066
Compressed air	m3/wafer	0.012	0.018	0.018	0.018	0.018	0.018
DI-water	kg/wafer	0.497	0.745	0.745	0.745	0.745	0.745
Process yield		0.999	0.998	0.998	0.998	0.998	0.998

Table A3
Emitter formation/diffusion – Main input parameters.

Input	**Unit**	**Ref-cSi**
Phosphoryl chloride	g/wafer	0.038
Phosphoric acid	g/wafer	0.183
Argon	g/wafer	0.614
Oxygen	g/wafer	2.436
Nitrogen	g/wafer	44.291
Propane	MJ/wafer	0.1139
Electricity	kWh/wafer	0.0310
Process yield		0.999

Table A4
PECVD – Main input parameters.

Input	Unit	Ref-cSi	Ref-SHJ	PVD-SHJ	NE-SHJ	ALD-SHJ	IBC-SHJ
Silane	g/wafer	0.029	0.039	0.039	0.102	0.020	0.059
Hydrogen	g/wafer		0.059	0.059	0.153	0.029	0.088
Oxygen	g/wafer		0.006	0.006	0.017	0.003	0.009
Ammonia	kg/wafer	0.000					
Shadow-Mask	pc/wafer						0.001
Electricity	kWh/wafer	0.080	0.160	0.160	0.174	0.080	0.240
Cooling water	L/wafer	4.79	9.59	9.59	10.93	4.79	14.38
Process yield		0.999	0.999	0.999	0.999	0.999	0.972

Table A5
ALD – Main input parameters.

Input	Unit	ALD-SHJ
TMA	g/wafer	0.0046
Oxygen	g/wafer	0.2090
Nitrogen	g/wafer	0.0027
Electricity	kWh/wafer	0.0069
Cooling water	L/wafer	0.5523
Process yield		0.9994

Table A6
TCO sputtering – Main input parameters.

Input	Unit	Ref-SHJ	PVD-SHJ	NE-SHJ	ALD-SHJ	IBC-SHJ
ITO target	g/wafer	0.0317	0.0317	0.0158	0.0158	0.0158
ZnO target	g/wafer				0.0263	
Shadow-Mask	pc/wafer					0.0003
Electricity	kWh/wafer	0.1506	0.1506	0.1506	0.1506	0.1506
Cooling water	L/wafer	12.232	12.232	12.232	12.232	12.232
Process yield		0.999	0.999	0.999	0.999	0.974

Table A7
Metallization – Main input parameters.

Input	Unit	Ref-cSi	Ref-SHJ	PVD-SHJ	NE-SHJ	ALD-SHJ	IBC-SHJ
Silver paste	g/wafer	0.167					
Silver paste low temp	g/wafer		0.500	0.250	0.250	0.250	
Al paste	g/wafer	1.400					
Ag target	g/wafer			0.069	0.069	0.069	0.138
Electricity	kWh/wafer	0.013	0.013	0.088	0.088	0.088	0.075
Compressed air	m3/wafer	0.027	0.027	0.027	0.027	0.027	
Process yield		0.997	0.997	0.998	0.997	0.997	0.973

Table A8
Module assembly – Main input parameters.

Input	Unit	Ref-cSi	Ref-SHJ	PVD-SHJ	NE-SHJ	ALD-SHJ	IBC-SHJ
Conductive adhesive	g/module		3.60	3.60	3.60	3.60	1.80
Standard backsheet	m^2/module	1.63					
HIT backsheet	m^2/module		1.63	1.63	1.63	1.63	
IBC backsheet	m^2/module						1.63
EVA	m^2/module	3.27	3.27	3.27	3.27	3.27	3.27
Glass	m^2/module	1.63	1.63	1.63	1.63	1.63	1.63
J-Box	pc/module	1.0	1.0	1.0	1.0	1.0	1.0
Stringing/tabbing	pc/module	1.0	1.0	1.0	1.0	1.0	1.0
Frame	pc/module	1.0	1.0	1.0	1.0	1.0	1.0
Electricity	kWh/module	3.00	3.00	3.00	3.00	3.00	3.00
Process yield		0.974	0.974	0.974	0.974	0.974	0.974

Table A9
Prices of input consumables.

Consumable	Price (USD)	Unit	Source
Acetic acid	0.51	kg	[68]
Aluminium frame	13.48	module	Market survey
Aluminium paste	0.052	g	[69]
Aluminium target	0.10	g	Own calculations
Ammonia	9.50	kg	Market survey
Argon	0.22	kg	[69]
Backsheet, HIT	7.00	m^2	Own estimate
Backsheet, standard	5.03	m^2	Market survey
Backsheet, structured IBC	10.00	m^2	[47]
Boron trifluoride	4.42	g	[70]
Calcium chloride	1.00	kg	Own estimate
Compressed air	0.02	m^3	[69]
Conductive adhesive	1.04	g	[47]
Cooling water	0.24	m^3	[69]
Cu paste	0.59	g	Own calculations
Cu paste HT	0.43	g	Own calculations
Cu plate solution	3.7	L	Own calculations
Cu target	0.05	g	Own calculations
DI-water	3.0	m^3	[69]
Electricity, general	0.10	kWh	Own estimate, for cell and module production
Electricity, hydro	0.025	kWh	Own estimate, for silicon production
Electricity, cogen	0.07	kWh	Own estimate, for silicon production
Ethanol	10.00	kg	Own estimate
EVA	1.85	m^2	Market survey
Fluid waste treatment	0.02	L	Own estimate
Hydrochloric acid	6.2	kg	[69]
Hydrogen	1.4	kg	[69]
Hydrogen fluoride	1.08	kg	[68]
Hydrogen peroxide	1.48	kg	[68]
Isopropanol	10.65	kg	[71]
ITO target	0.85	g	Own calculations
J-Box	6.50	piece	[18]
Monocrystalline silicon wafer	1.03	piece	Own calculations
Nickel plate solution	0.05	mL	Own calculations
Nitric acid	0.23	kg	[68]
Nitrogen	0.28	kg	[69]
Oxygen	0.65	kg	[69]
Phosphoryl chloride	450	kg	[69]
Propane	0.011	MJ	[72]
Shadow-Mask	100	piece	Own estimate
Silane	0.070	g	[69]
Silver paste	0.82	g	Own calculations[a]
Silver paste low temp	1.06	g	Own calculations[b]
Silver plate solution	0.085	mL	Own calculations
Silver target	0.89	g	Own calculations
Sodium hydroxide	1.94	kg	[68]
Sodium silicate	0.50	kg	Own estimate
Solar glass	5.5	m^2	Market survey
Solvents	10.00	kg	Own estimate
Stringing/tabbing and bussing ribbons	2.50	module	[18]
Titanium dioxide	2.26	kg	[68]
Trimethyl aluminium (TMA)	2.3	g	[73]
ZnO target	0.05	g	[71]

[a] Based on silver content of 60%, silver price and paste price in [18].
[b] Based on silver content of 80%, silver price and paste price in [18].

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